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Conference Coverage

ESL – where we're at and where we're going

By Bill Murray

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Gary Smith of [GarySmithEDA](#) presented a snapshot of the status and direction of electronic system level design (ESL) methodology at the recent Open SystemC Initiative (OSCI) SystemC Day at the Design and Verification Conference (DVCon 2010) in San Jose, California. He talked about the progress of ESL, its five high value applications, and market sizing, then concluded with some comments about its ability to satisfy the needs of the embedded system software developer.

Smith is a long-time observer of ESL design and verification, and a leading exponent of the need for electronic design automation (EDA) to extend itself into system design. For some years, he has exhorted the EDA community to pay more attention to the needs of embedded software developers, with the rallying cry of "It's the software, stupid!"

Smith said that ESL finally took off in 2004. "Our survey that year showed significant use of ESL, albeit often with in-house, proprietary C/C++ tools. Our survey two years later showed that, of the engineers who could be expected to benefit from the use of ESL methodologies, about four percent were actually using it. This year, it's about five percent. It's not growing greatly – but it is growing. Remember that the shift to RTL took about eight years – if ESL pans out the same way, it should be done by 2012." See figure 1.

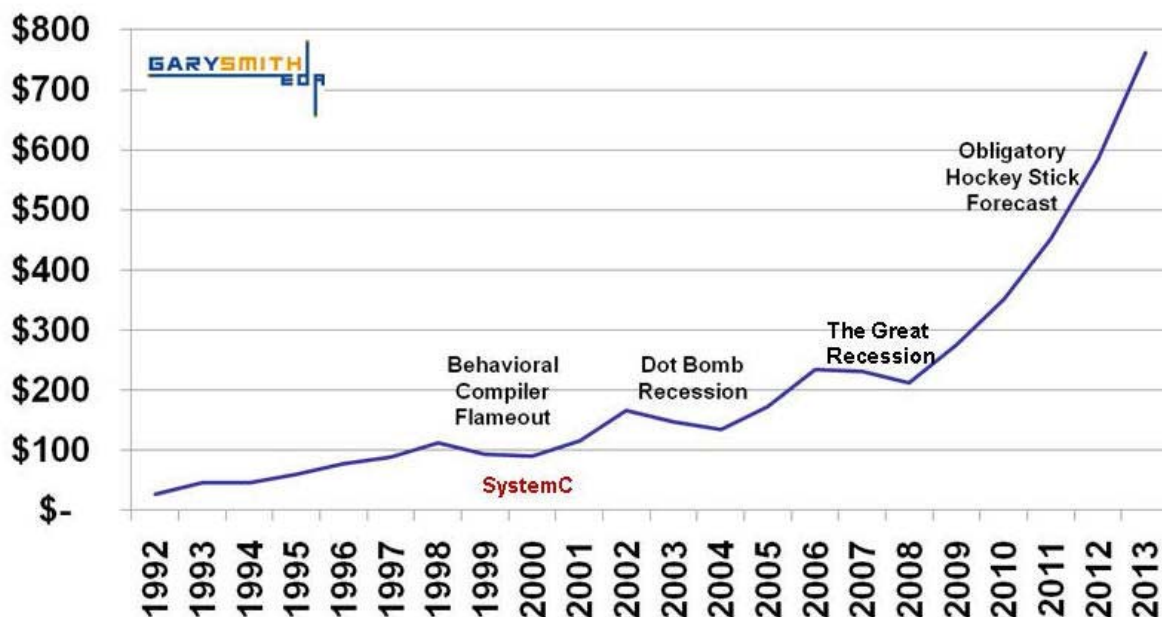


Figure 1: Annual ESL revenue (Source: GarySmithEDA)

On methodology, Smith said "Hardware design and verification methodology is firming up, and the hardware tool flow is filling out. But software development methodology is still up in the air, and the software tool flow needs development."

Two down, three to go

Smith said "We have two killer apps down. One is ESL synthesis. Mentor already has a solid market position with Catapult C, and they've just enhanced it with SystemC support – they'll be hard to beat. The other one is the software virtual prototype. Synopsys has just bought nearly everyone, but Carbon and Imperas remain."

"We're in trouble on SoC design costs, and it's primarily on the software side," Smith said (see figure 2). "We'd like to see hardware development under \$20M, and the same for software. At that point, we can revitalize the fabless semiconductor business. Virtualization seems to be the answer. The key to the hardware cost issue is going to be the silicon virtual prototype – which Cadence and Atrenta are working on. This is going to be the RTL handoff, and we could go back to the ASIC model of the 1980's, where the designers hand-off their functional design to the silicon manufacturer for silicon implementation."

So, said Smith, the three to go are "First, the architect's workbench, which MathWorks, Mentor and Cofluent are working on." He continued "Second is thin virtualization and network on chip. The real time operating system (RTOS) is far too fat for on-chip applications, so we need to thin it to support many-core design and its associated hardware accelerators – this will also be critical to low power design. The result will be the new RTOS for many-core designs."

"The third is embedded software automation (ESA), a term coined by Mentor's Wally Rhines," said Smith. "Up to ten new tools may be needed for this task, and some of them will be ESL killer apps."

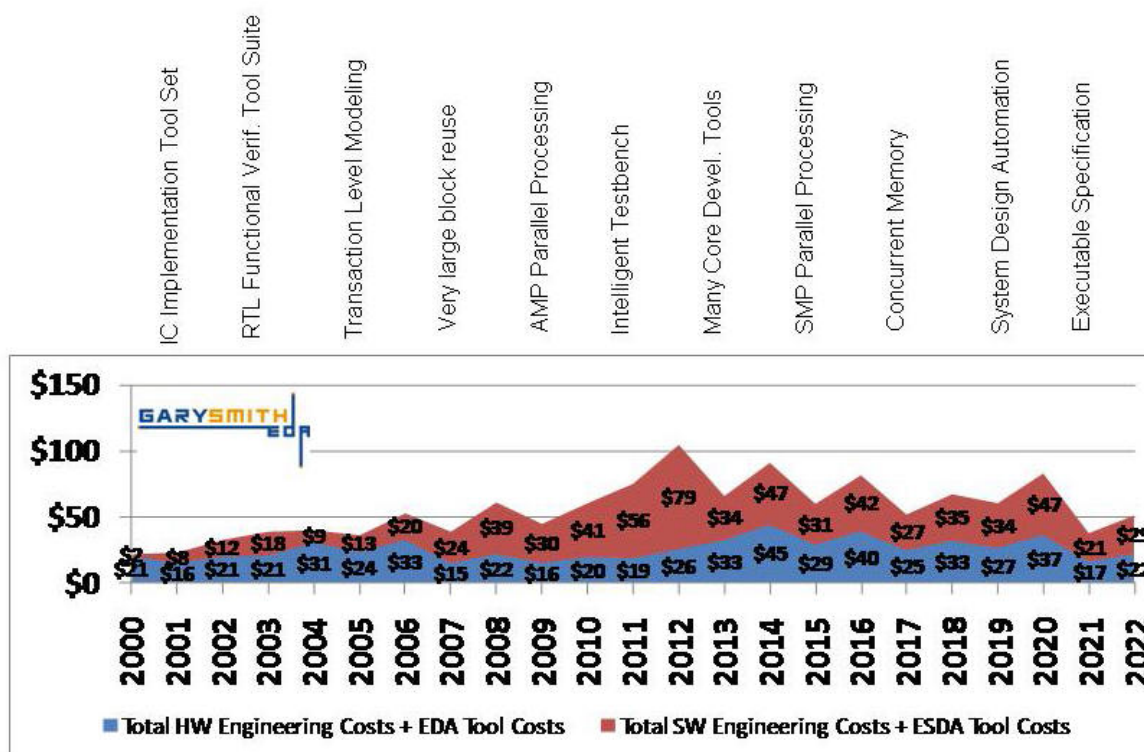


Figure 2: ITRS cost chart 2009; millions of dollars (Source: GarySmithEDA)

Three killer apps

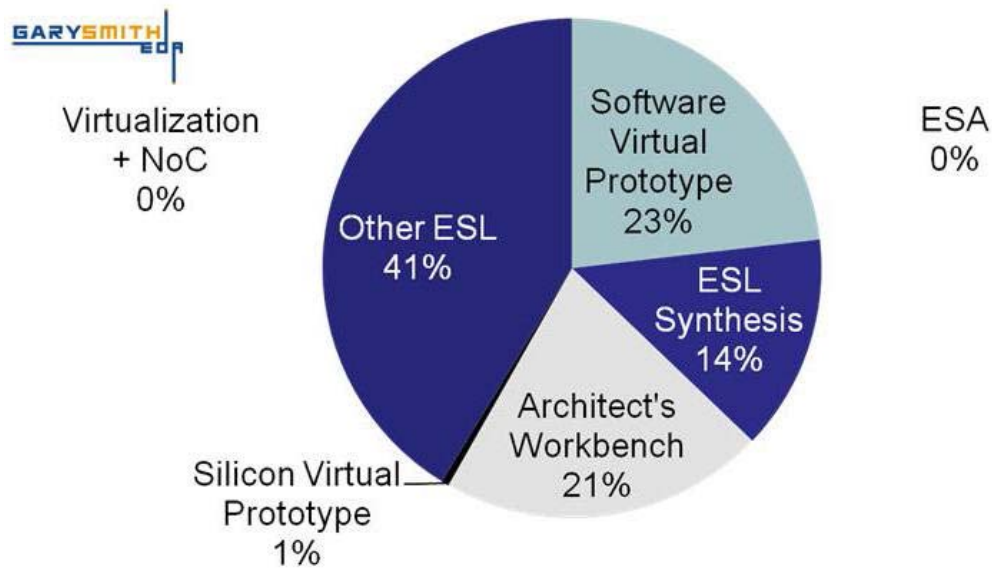


Figure 3: The ESL killer applications and their market shares (Source: GarySmithEDA)

User groups and market size

Smith said "We have four user groups. First the system architects. There used to be one architect working on a mobile phone, now there are six, and each of them has a modeling and 'what-if?' analysis team. This is becoming a significant effort for the system builders. Then there are the SoC system designers who use SystemC, and the board-level system designers, who use C/C++. Then there's the largest group, the embedded system software developers."

"Looking at seats, you can really see the difference," he said (see figure 4). "SoC design has the fewest seats. That doesn't mean that it is the smallest market because the average selling prices are higher. The board design guys are slightly more numerous than the SoC guys – we fall down on our knees and pray that their seats will be about \$120K each."

"Then there are the software developers. If we can get them up to \$40K per seat [with new ESA tools and methodologies], there would be an \$8B ESL market. The fear of free software development tools is receding because the software guys haven't figured out the parallel processing problem. Multicore software development tools are going to be very different from the single-processor software development tool. The new tools are not going to be a free download."

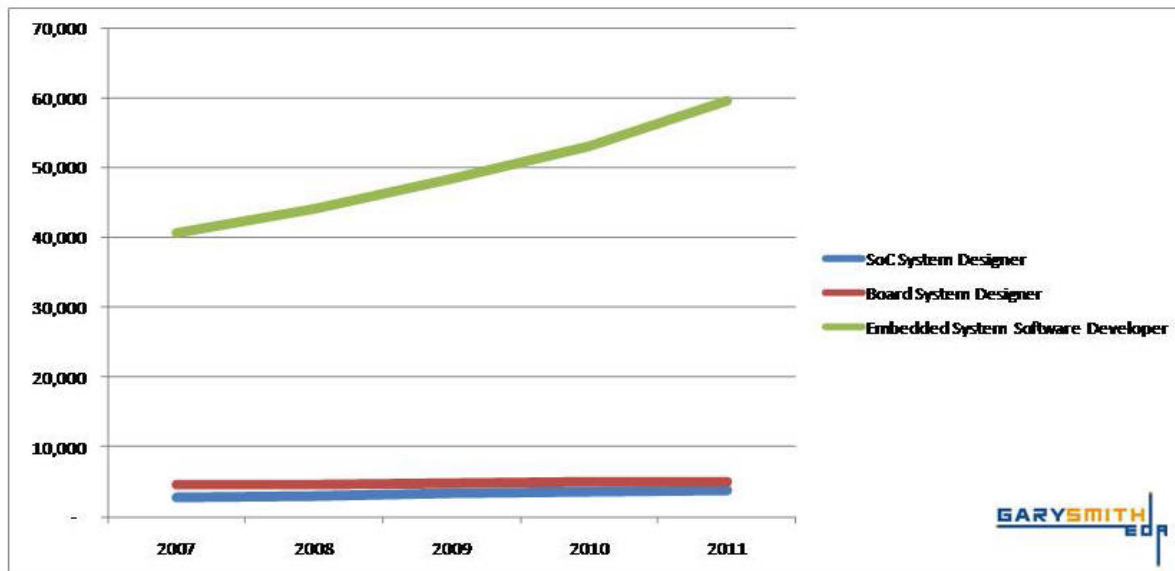


Figure 4: ESL design and verification seats (Source: GarySmithEDA)

Gary's SystemC wish list

"We need a behavioral-level SystemC standard," said Smith. "IBM and Intel have been pushing this for some time. The system design guys need a modeling technology that is more accurate than what you get from C or M. What you get out of M is a good idea and some stud code. We need something more than stud code, although it doesn't have to be final code. And it doesn't have to be push-button."

"We need a more robust SystemC testbench library. In its current state, I would not recommend anyone to rely on it. It really needs work – we don't want ten different languages to get a design out of the door."

"We need SystemC support for embedded parallel processing software development. I'm not saying that software guys should use SystemC, but we need SystemC constructs that are more software-friendly. We need an information flow that makes it easier for the software guys to get closer to the hardware."

Audience questions

How many architects are there? Smith said "We've done no surveys recently. We studied this for Cadence in the late Nineties and came up with a number of 400. We couldn't convince Cadence that this number would grow dramatically."

Where do you see ESL verification going? Smith said "Most of the 'Other 41 percent' is ESL verification. A lot of the future ESL embedded software design tools will be verification software. The software guys have a lot of verification problems like you wouldn't believe. Chip designers verify; software developers test."

Why should I choose SystemC over SystemVerilog at the architectural level? Smith said "What SystemVerilog has that we must get into ESL test languages is assertions – but it must be at the transaction level. SystemVerilog is an RTL language, and has never made it into ESL. It has no concept of software whatsoever – it doesn't fit into a flow that's all about software."

Do you see an ESL IP industry emerging? Smith said "In our ITRS cost analysis, we found that standard RTL blocks over a million gates were basically unusable by the end-customer. They were looking for modifiable blocks that can be dis-assembled and re-assembled without losing too much of the verification understanding. That must be done at the transaction level, albeit with RTL models below

that. The IP providers need to move up to the transaction level – without it, you won't play in the IP game very much longer.”

Further Reading

[ESL Models and their Application](#). Book by B. Bailey and G. Martin. Published by Springer Verlag.

[ESL Design and Verification](#). Book by B. Bailey, G. Martin & A. Piziali. Published by Elsevier.

[Virtual platforms – a reality check, part 1](#)

[Virtual platforms – a reality check, part 2](#)

[OSCI TLM-2 proposal – the debate begins](#)

[SystemC extensions take AMS to the system level](#)

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